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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,797	08/02/2001	Jonathan Lamb	SEMT-025	7401

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EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,797	LAMB ET AL.	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 -24, 26 - 30, 32, and 35* is/are allowed.

6)☒ Claim(s) *1-18,25,36,37,40,45,46 and 49* is/are rejected.

7)☒ Claim(s) *31, 33, 34, 38, 39, 41 - 44, 47, 48, and 50 - 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 31,33, and 34 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 25 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claim 25, the applicant is claiming that second multiplexer selection control signal is coupled to at least the Q-output of the D-type flip-flop circuit. However, the specification discloses that the Q-output of the second D-type flip-flop is coupled to the B-input of the divider 412.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Brilman et al (US Patent 4,663,631).

Regarding claim 1, Brilman et al teach having a first phase detector 15 and second phase detector 9 receiving two inputs and outputting a control signal PLL-x and PLL-y respectively (see figure 1). Further a control unit 3 receiving first control signal (PLL-x), second control signal (PLL-y), first gain factor (AGC-x) and second gain factor (AGC-y), and outputting a phase measurement resultant signal (see figure 1 component 2).

Regarding claim 2, Brilman et al teach first control signal (PLL-x) enabling the the application of the first gain factor (AGC-x) and second control signal (PLL-y) enabling the second gain factor (AGC-y).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 – 7, 10 – 14 and 17 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brilman et al (US patent 4,663,631) in view of Dosho et al (USPAP No: US 2001/0007436)

Regarding claims 3 –7, 10 – 14 and 17 – 18, Brilman et al is cited as explained in the above paragraph. Brilman el at failed to teach a phase detector includes the two registers and a NAND-gate a synchronizing circuit receiving a first phase indicator signal and a second phase indicator signal and outputting a first synchronized phase indicator signal and second synchronized phase indicator signal. However, Dosho et al teach a synchronizing circuit receiving signal from the phase detector and outputting at least two output signals (see Figure 2). It would be obvious to an ordinary skilled in the art at the time the invention was made to substitute Dosho's phase detector and the synchronizing circuit with Brilman's phase detector to enhance the efficiency of the phase detector.

Regarding claim 3, Dosho et al teach that a phase detector with synchronizing circuit (see figure 2).

Regarding claim 4, with limitations of claim 3, Dosho et al also teach that the phase detector includes two registers and a NAND-gate circuit (see figurer 2).

Regarding claim 5, with the limitations of claim 4, Dosho et al teach the first and second registers receive first input source (R in figure 2), second input source (V in figure 2) respectively and reset control signal (RST in figure 2) ands outputting first and second phase indicator signal (VU and VD) respectively. The NAND-gate circuit receives VU and VD and outputting the reset control signal.

Regarding claim 6, with the limitations of claim 5, Dosho et al also teach the first input (R) source is coupled to the clk-input of the DFF circuit, the reset control signal (RST) is coupled to the reset-input off the DFF and the first phase indicator signal (VU) coupled to the Q-output of the DFF circuit.

Regarding claim 7, with the limitations of claim 5, Dosho et al also teach the first input (V) source is coupled to the clk-input of the DFF circuit, the reset control signal (RST) is coupled to the reset-input off the DFF and the first phase indicator signal (VD) coupled to the Q-output of the DFF circuit.

Regarding claim 10, with the limitations of claim 3, Dosho et al teach that the synchronizing circuit includes a first register (60 in figure 2) and second register (61 in figure 2).

Regarding claim 11, with the limitations of claim 10, Dosho et al teach that the first register having D-input, a clk-input, and a Q-input; the first phase indicator signal (VU) is coupled to the D-input, the clock input is coupled to the clk-input and the first synchronized phase indicator signal (SU) is coupled to the Q-output of the DFF circuit.

Regarding claim 12, with the limitations of claim 10, Dosho et al teach that the second register having D-input, a clock-input, and a Q-input; the second phase indicator signal (VD) is coupled to the D-input, the clock input is coupled to the clock-input and the first synchronized phase indicator signal (SD) is coupled to the Q-output of the DFF circuit.

Regarding claim 13 – 14 and 17 – 18, the phase indicator signal is activated upon detection of the transition edge is inherent in the basic operation of D-type flip-flop.

Claims 8 – 9, 15 – 16, 36 – 37, 40, 45 – 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brilman et al (US Patent 4,663,631) in view of Dasho et al (USPAP US 2001/0007436) as applied to claim 3 above, and further in view of DuFour (US patent 6,229,864 B1).

Regarding claims 8 – 9, 15 – 16, 36 – 37, 40, 45 – 46 and 49, Brilman et al does not teach that the second phase detector includes a D-type flip-flop circuit having a D-input, a clock input and a Q-output. However, DuFour teaches a phase detector having a D-type flip-flop (see figure 2). It would be obvious to an ordinary skilled in the art to use DuFour's phase detector instead of Brilman's phase detector to benefit simpler design.

Regarding claim 8 and 9, with the limitation of claim 3, DuFour teaches that phase detector includes a D-type filp-flop and having the first input coupled to the clock-input and the second source coupled to the D-input and the order indicating signal coupled to the Q-output of the DFF circuit.

Regarding claim 15 and 16, the order indicator signal is activated upon detection of the transition edge is inherent in the basic operation of D-type flip-flop.

Claims 36, 37, 40, 45, 46, and 49 inherits the limitation of claim 3 further; DuFour teach a phase detector includes a D-type filp-flop and having the first input coupled to the clock-input and the second source coupled to the D-input and the order indicating signal coupled to the Q-output of the DFF circuit.

Allowable Subject Matter

Claims 19 – 24, 26 – 30, 32, and 35 are allowed.

Claims 38 – 39, 41 – 44, 47 – 48, and 50 – 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The applicant recites a control unit include a synchronous signal latch, a first multiplexer, an edge detection block, a first register, a second register, a programmable storage unit, a second multiplexer, and a divider. The prior art does not teach a control unit with components mentioned above. Therefore, the claims 19 – 24, 26 – 30, 32 and 34 are allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
Patent Examiner

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